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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/781,477
Filing Date: February 17, 2004
Appellant(s): MARTINEZ ET AL.

Nenad Pejic
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed December 13, 2007 appealing from the Office Action mailed February 14, 2007.

(1) Real Party in Interest99

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,732,298	Murthy	5-2004

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Murthy US Patent 6,732,298.

Detailed action

Claims 1-30 have been presented for examination.

Claims 1-30 have been rejected

Objection

Claim 21 recites "The system of claim 21", it appears that claim 21 depends from claim 20. Correction is highly suggested.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Murthy US Patent 6,732,298.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in

the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In regard to claim 1,

Murthy discloses a method of reboot reporting comprising:

- Reading a plurality of input lines associated with a plurality of computer systems having a plurality of processors;(Figure 1; items 10A,10B,10C,10D)
- Generating at least one non-maskable interrupt signal; (Column 2; lines 61-62)
- Outputting the non-maskable interrupt signal to a processor of the plurality of computer systems; (Column 2; lines 63-64) [When the nonmaskable pseudo interrupt **informs** it is being outputted to the processor]
- Outputting the non-maskable interrupt signal to a manager associated with the plurality of computer systems; (Column 4; lines 18-21) [Murthy disclose "that if it is desired for the computer system to have a dedicated display device …a video graphic controller would interface the display device to the system. The display may comprise any suitable electronic display device upon which any image or text can be represented." Examiner considers the display as a mean for outputting the non-maskable interrupt to a manager because a manager needs a display terminal to receive this outputs]

- Generating an indication that at least one computer system has a fault condition. (Column 2; lines 63-65) [Examiner considers informing the processor that the array controller board is inoperative as an indication of a fault]

In regard to claim 2,

Murthy discloses the method of claim 1 further comprising associating the non-maskable interrupt signal with at least one computer system of the plurality of computer systems.(Figure1; items 50A,50B,50C) [this is where the NMI happens]

In regard to claim 3,

Murthy discloses the method of claim 2 further comprising generating a notice identifying the at least one computer system.(Column 6; lines 46-52) [debugging with the NMI means first that the item to be debugged is identified before starting the debugging.]

In regard to claim 4,

Murthy discloses the method of claim 3 further comprising redistributing the processing load from the at least one computer system to the remaining plurality of computer systems. (Column 8; lines 17-21) [because the remainder of system 100 is not effected it means that the system has a redistribution system in case a fault happens in one of its elements.]

In regard to claim 5,

Murthy discloses the method of claim 1 further comprising counting the number of times the non-maskable interrupt signal is generated. (Column 4; lines 36-39) [Examiner considers the LPC as a pin that counts the NMIs]

In regard to claim 6,

Murthy discloses a system for reboot reporting comprising:

- a plurality of computer systems having at least one processor and at least one non-maskable interrupt output;(Figure 1; items 50A,50B,50C) and (Figure 2; item 50) and (Column 2; lines 63-65)
- a manager system in circuit communication with the plurality of computer systems and comprising at least one non-maskable interrupt input associated with the plurality of computer systems. (Column 4; lines 18-21) [Murthy disclose "that if it is desired for the computer system to have a dedicated display device ...a video graphic controller would interface the display device to the system. The display may comprise any suitable electronic display device upon which any image or text can be represented." Examiner considers the display as a mean for outputting the non-maskable interrupt to a manager because a manager needs a display terminal to receive this outputs]

In regard to claim 7,

Murthy discloses the system of claim 6 wherein the plurality of computer systems comprises a plurality of non-maskable interrupt outputs (Figure 1; items 50A,50B,

50C) [each controller can generate an interrupt] and the manager system comprises a plurality of non-maskable interrupt inputs (Column 4; line 26) [Examiner considers when any image or text can be dislayed that means that the manger receives plurality of NMI].

In regard to claim 8,

Murthy discloses the system of claim 7 wherein the non-maskable interrupt outputs of the plurality of computer systems are in circuit communication with the plurality of non-maskable inputs of the manager system. (Figure 1; item 20) [PCI couples item 50 to item 22 and item 28 where it is possible to locate the display considered as manger as demonstrated before].

In regard to claim 9,

Murthy discloses the system of claim 6 wherein the plurality of computer systems comprises

- least one computer system having a processor, (Figure 1; item 10)
- a first bridge circuit (Figure 2; item 54)
- second bridge circuit and wherein the second bridge circuit comprising a non-maskable interrupt signal output in circuit communication with the processor (Figure 2; item 64).

In regard to claim 10,

Murthy discloses the system of claim 9 wherein the non-maskable interrupt output of the second bridge is in circuit communication with the manager system. (Figure 2) [Figure shows that item 64 is coupled to item 54 through PCI 56 which in turn is connected to the rest of the system with PCI 20, PCI 20 is coupled to LPC24, and ends item 28 where it is possible to locate the display considered as manger as demonstrated before].

In regard to claim 11,

Murthy discloses the system of claim 6 further comprising logic for reading at least one non-maskable interrupt input associated with the plurality of computer systems.(Column 3; lines 5-8)

In regard to claim 12,

Murthy disclose the system of claim 11 further comprising logic for generating an indication that at least one computer system has a fault condition based on the presence of a non-maskable interrupt signal present on the at least one non-maskable interrupt input. (Column 3; lines 9-10)

In regard to claim 13,

Murthy discloses a system for reboot reporting comprising:

- a plurality of computers; (Figure 1; item 10)

- means for managing the plurality of computers;(Column 3; lines 66-67) and (Column 4; lines 1-6)
- and means for outputting a non-maskable interrupt signal indicating a fault condition associated with at least one of the plurality of computers to the means for managing. (Column 2; lines 63-64) [When the nonmaskable pseudo interrupt **informs** it is being outputted to the processor]

In regard to claim 14

Murthy discloses the system of claim 13 further comprising means for detecting the non-maskable interrupt signal indicating a fault condition associated with at least one of the plurality of computers and generating a detection signal in response thereto. (Column 3; lines 9-10)

In regard to claim 15,

Murthy discloses the system of claim 13 further comprising means for generating at least one non-maskable interrupt signal. (Column 2; lines 61-62)

In regard to claim 16,

Murthy discloses the system of claim 13 further comprising means for generating an indication that at least one computer has a fault condition. (Column 2; lines 63-65) [Examiner considers informing the processor that the array controller board is inoperative as an indication of a fault]

In regard to claim 17,

Murthy discloses the system of claim 13 further comprising means for associating the non-maskable interrupt signal with at least one computer of the plurality of computers. (Figure1; items 50A, 50B, 50C) [This is where the NMI happens]

In regard to claim 18,

Murthy discloses the system of claim 17 further comprising means for redistributing the processing load from the at least one computer to the remaining plurality of computers. (Column 8; lines 17-21) [Because the remainder of system 100 is not effected it means that the system has a redistribution system in case a fault happens in one of its elements.]

In regard to claim 19,

Murthy discloses the method of claim 13 further comprising means for counting the number of times the non-maskable interrupt signal is generated. (Column 4; lines 36-39) [Examiner considers the LPC as a pin that counts the NMIs]

In regard to claim 20,

Murthy discloses a computer system comprising:

- a processor; (Figure 2; item 58)
- a memory; (Figure 2; items 60 & 50)

- at least one bridge circuit in circuit communication with the processor;(Figure 2; item 64)

- a non-maskable interrupt signal circuit in circuit communication with the processor and at least one other computer system.(Figure 2;item 59)

In regard to claim 21,

Murthy discloses the system of claim 21 wherein the at least one other computer system comprises an enclosure manager. (Column 4; lines 18-21) [Murthy discloses "that if it is desired for the computer system to have a dedicated display device …a video graphic controller would interface the display device to the system. The display may comprise any suitable electronic display device upon which any image or text can be represented." Examiner considers the display as a mean for outputting the non-maskable interrupt to a manager because a manager needs a display terminal to receive this outputs and it is enclosed]

In regard to claim 22,

Murthy disclose system comprising:

- an enclosure having a plurality of individual computer systems and a manager computer system;(Column 3; line 56) [A server is an enclosure]

- wherein at least one of the plurality of computer systems comprises a processor and a non-maskable interrupt signal circuit, the non-maskable interrupt signal

circuit in communication with the processor and the manager computer system,(Figure 2; items 58,59 and PCI 56 and 20 and item 28 of figure 1)

- the non-maskable interrupt signal circuit comprising a bridge circuit and a non-maskable interrupt signal path to the processor and the manager computer system. (Figure 2; item 64; and PCI 56 and 20)

In regard to claim 23,

Murthy discloses the system of claim 22 wherein the manager computer system comprises a non-maskable interrupt signal input. (Column 4; lines 25-26) [Because the display manager contains a text that will display an NMI message, his message has to come from an input]

In regard to claim 24,

Murthy discloses the system of claim 23 wherein the manager computer system comprises logic for reading a state of the non-maskable interrupt signal input. (Column 3; lines 5-8)

In regard to claim 25,

Murthy discloses the system of claim 24 wherein the manager computer system comprises logic for generating a notice based on the state of the of the read non-maskable interrupt signal input. (Column 4; line 26) [the text message is considered as a notice]

In regard to claim 26,

Murthy discloses a system comprising:

- Means for housing a plurality of digital devices; (Figure 1; item 100)
- Means for managing the plurality of digital devices,(Column 3 and 4; lines 66-67, lines 1-5)
- Means for managing comprising a location within said means for housing;(Figure 1; item 28)
- Means for receiving and processing executable instructions,(Figure 2; item 58)
- Means for receiving and processing comprising a location within said means for housing; (Figure 1; item 22)
- Means for generating a non-maskable interrupt signal; (Figure 2; item 50)
- Means for communicating the non-maskable interrupt signal to the means for receiving and processing and to the means for managing. (Figure 2; items 56 & 20)

In regard to claim 27,

Murthy discloses the system of claim 26 wherein the means for communicating the non-maskable interrupt signal to the means for receiving and processing and to the means

for managing comprising a non-maskable interrupt signal pathway. (Figure 2; items 56 & 20)

In regard to claim 28,

Murthy discloses the system of claim 26 wherein the means for managing the plurality of digital devices comprises means for reading the state of the means for communicating and means for generating a notice based on the state of the means for communicating. (Column 3; line 8) and (Figure 2; item 64)

In regard to claim 29,

Murthy discloses the system of claim 26 wherein the means for managing the plurality of digital devices comprises means for redistributing a processing distribution among the plurality of digital devices. (Column 8; lines 17-21) [because the remainder of system 100 is not effected it means that the system has a redistribution system in case a fault happens in one of its elements.]

In regard to claim 30,

Murthy discloses the system of claim 26 wherein

the means for generating a non-maskable interrupt signal comprises a bridge circuit associated with the means for receiving and processing. (Figure 2; item 64) and (Figure 1; item 22 and 28)

(10) Response to Argument

Appelant's arguments with respect to claims 1 and 5 have been considered but are not persuasive. Please refer to the above section of (9) Grounds of Rejection for details. In regard the first argument which states "Therefore, it is respectfully submitted that the 102 rejection of the independent claims cannot be sustained because Murthy expressly discloses that its processor does not implement non-maskable interrupts" Examiner respectfully disagrees. Examiner will explain why Murthy disclosed in the abstract of Patent 6,732,298, that the processor does not implement non-maskable interrupts. It essential to know that Murthy's invention comes to overcome the problem of not being able to implement non-maskable interrupts, by finding a way to implement them. To this purpose Figure 2 is a very important Figure. This figure shows two important elements. The first element is processor 58 , and the second element is bridge 64. These two elements in combination give the system, and precisely processor 58, the capability of generating and processing non-maskable interrupts. The evidence that supports this reasoning is clear when Murthy discloses in Column 6 "In conventional systems, connection of a test device to a port connector 70A or 70B automatically asserts an interrupt to processor 58. This interrupt will cause the system to enter a test mode to permit debugging to occur. If however, the interrupts have been disabled, connection of the test device will not work. As will be explained below, the preferred embodiment of the invention uses a machine check exception ("MCP") signal 61 to solve this problem. The MCP line normally functions as a critical failure signal to inform processor 58 of a catastrophic failure on the hardware board (e.g. chip is inoperable, interconnects between chips have been shorted together or are open so

board is inoperative). The result is that a processor 58 that has no equivalent to a non-maskable interrupt (NMI) (a NMI is an interrupt which cannot be disabled) capability is effectively given such a capability"

The fact that Murthy called these non-maskable interrupts non maskable pseudo interrupt is irrelevant to the argument stated above by the Applicant, because an interrupt when implemented is an interrupt whether it is called pseudo or something else. In other words, a result of implementing interrupts or pseudo interrupts within a processor is the same. The result is to call an exception, and execute an exception routine as demonstrated by the above passage. Applicant's argument is based on very weak evidence, not a solid reasoning, and a misunderstanding of how interrupts work within a processor. The argument is not valid.

In regard the second argument which states "In particular, the Final Rejection states that "The Examiner considers the listing of int0, int1, int2, as counting interrupts" The listing in the cited Murthy disclosure is clearly a reference to the structure, and is not a process step of "counting the number of times the NMI signal is generated." Hence, it is respectfully that the relied upon disclosure does not teach or suggest the "counting...." Limitation of dependent claim 5. "

Examiner respectfully disagrees. Examiner will explain how the limitation of claim 5 is met by Murthy. First, it is important to mention that the interrupts Murthy talks about are hardware interrupts, this means that when one a hardware element like a bus or bridge enters a faulty environment an interrupt is generated. Figure 2 shows clearly that an interrupt is generated at SCSI 66 level labeled int0, the same Figure shows an interrupt

is generated at SCSI 66 (different than the first one) level labeled int1, and finally the same Figure shows an interrupt at PCI TO PCI BRIDGE 54 level labeled int2. It is evident that while Murthy labels the generated interrupts as int0, int1, int2, Murthy also counts the interrupts by counting the label 0,1,2. Additionally, as a support to the Examiner position, Examiner turns to Column 7 where Murthy discloses "Assertion of a general hardware device interrupt causes the corresponding bit to be set for that particular interrupt in the interrupt status register 80 in the processor-to-PCI bridge 64. Once a bit in the interrupt status register is set, the bridge 64 generates int 59 (*) to the processor to indicate to the processor the occurrence of **one or more hardware device interrupts**" This indication solidifies the position taken by the Examiner previously. Further, Murthy discloses in Column 3 "Inasmuch as computer system 100 is preferably a server system, the computer system 100 preferably comprises multiple CPUs 10A, 10B, 10C, 10D arranged as shown in a configuration to permit simultaneous, multi-tasking to occur. The CPUs may comprise, for example, Pentium.RTM. III processors from Intel Corp., or other suitable processors." Additionally, Column 5 discloses "The processor 58 controls the operation of the disk array controller 50. The processor 58 may comprise a 700 Series PowerPC processor (e.g., model 740) manufactured by IBM Corp. However, **other microprocessors** or microcontrollers may be used as the array processor 58 and still be within the scope of this invention." Examiner concludes from this passage that a Pentium **III** is used to implement the invention disclosed by Murthy. Further research on the Pentium **III** lead the Examiner to a important document entitled "**Intel Architecture Software Devoloper's Manual Volumn 3: System Programming**

Guide" The part of this document that pertains to counting non-maskable interrupts is found on Appendix A-14, where the document shows a table under the title of "Events That Can Be Counted with the Pentium Processor Performance-Monitoring Counters" Under event 27H, Murthy lists HARDWARE INTERRUPTS, and describes it as number of taken INTR and NMI interrupts. For the record NMI stands for non-maskable interrupt. Applicant's argument is not valid.

(*) Examiner encourages the Applicant to distinguish the difference in the label used between int----63, int---59, and int0, int1, int2 [this distinction enforces the interrupt counting position taken by the Examiner]

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Amine Riad

/Amine Riad/ Examiner, Art Unit 2113

/Robert W. Beausoliel, Jr./

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